

IN THE CLAIMS:

Claim 1 (**currently amended**) A plurality of metal bumps for connecting a nonconducting substrate and a chip, comprising:

at least a first metal bump having a first sidewall, the first sidewall comprising a first predetermined area; and

at least a second metal bump separated from the first metal bump having a second sidewall, the second sidewall comprising a second predetermined area adjacent to the first predetermined area;

wherein the first predetermined area is covered with an insulating layer, and the second predetermined area is not covered by the insulating layer.

Claim 2 (**canceled**)

Claim 3 (**original**) The plurality of metal bumps of claim 1, wherein the second sidewall further comprises a third predetermined area outside the second predetermined area, and the third predetermined area is covered with an insulating layer.

Claim 4 (**original**) The plurality of metal bumps of claim 1, wherein the first sidewall is completely covered with an insulating layer.

Claim 5 (**canceled**)

Claim 6 **(original)** The plurality of metal bumps of claim 1, wherein the nonconducting substrate comprises a plurality of first metal pads, and the chip comprises a plurality of second metal pads which correspond to the first metal pads.

Claim 7 **(original)** The plurality of metal bumps of claim 6, wherein each metal bump is fixed between the first metal pad and the correspondent second metal pad.

Claim 8 **(original)** The plurality of metal bumps of claim 1, wherein the space between two adjacent metal bumps that are sandwiched by the nonconducting substrate and the chip is filled with an anisotropic conductive film (ACF).

Claim 9 **(original)** The plurality of metal bumps of claim 1, wherein each metal bump is fixed between the first metal pad and the correspondent second metal pad.

Claim 10 **(original)** The plurality of metal bumps of claim 1, wherein the insulating layer is made of silicon oxide or silicon nitride.

Claims 11 - 19 **(canceled)**